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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,825	07/23/2003	Christopher L. Hamlin	01-524/1C	9207

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,825	HAMLIN, CHRISTOPHER L.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 9, 15 and 22 are objected to:

In claims 1 and 9 the recitation of " a fabric interconnect" is not clear to what applicants intend to mean.

In claims 15 and 22 the recitation of " a fabric" is not clear to what applicants intend to mean.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being unpatentable by Athanas et al. (US Patent 5,828,858).

As to claims 1, 9, 15 and 22 Athanas discloses:

(1) A system for providing distributed dynamic functionality in an electronic environment comprising (col.10, ll.23-67; col.11, ll.1-11):

a plurality of platforms (configurable functional units/IFU/FU), the platforms suitable for providing a logic function, the platforms including embedded programmable logic (programmable arithmetic unit/ALU), memory (input registers) and a reconfigurable

core (barrel shifter/output delays), the logic, memory and reconfigurable core communicatively coupled via a fabric interconnect (col.2, ll.26-38; col.8, ll.12-42); and

a map expressing logic functions of the plurality of platforms (col.3, ll.58-67; col.4, ll.1-67; col.5, ll.1-2; col.8, ll.9-12),

wherein the platforms and the map are used for integrated circuit design (configuration) (col.1, ll.53-67; col.2, ll.1-2; col.6, ll.32-38; col.7, ll.40-57);

(9) A method for providing an executable suitable for being employed by a plurality of platforms, comprising (col.10, ll.23-67; col.11, ll.1-11):

receiving a program of instructions (programming information) (col.3, ll.1-14);

determining availability of a plurality of platform for performing the program of instructions, the plurality of platforms including embedded programmable logic, memory and a reconfigurable core, the logic, memory and reconfigurable core communicatively coupled via a fabric interconnect that is isochronous, wherein availability of the platforms includes at least one of load value of the platform and functionality of the platforms (col.10, ll.23-67; col.11, ll.1-11; col.3, ll.15-22; col.4, ll.53-67; col.5, ll.1-2; col.8, ll.36-46; col.9, ll.34-49); and

translating (concatenation of a programming header and operand data) the program of instructions into an executable suitable for operation by the plurality of platforms based on the determined availability (col.4, ll.17-52; col.10, ll.53-67; col.11, ll.1-11),

wherein the plurality of platforms are used for integrated circuit design (col.1, ll.53-67; col.2, ll.1-2; col.6, ll.32-38; col.7, ll.40-57);

(15) A system for providing distributed dynamic functionality in an electronic environment comprising (col.10, ll.23-67; col.11, ll.1-11):

a plurality of platforms communicatively coupled via an isochronous fabric, the platforms suitable for providing a logic function, the platforms including embedded programmable logic, memory and a reconfigurable core communicatively coupled (col.2, ll.26-38; col.8, ll.12-46; col.9, ll.34-50); and

a map expressing availability of the plurality of platforms for performing a logic function (col.2, ll.54-67; col.3, ll.15-22; col.3, ll.58-67; col.4, ll.1-67; col.5, ll.1-2; col.8, ll.9-12; col.10, ll.53-67; col.11, ll.1-11),

wherein the platforms and the map are used for integrated circuit design (col.1, ll.53-67; col.2, ll.1-2; col.6, ll.32-38; col.7, ll.40-57);

(22) A system for providing distributed dynamic functionality in an electronic environment comprising (col.10, ll.23-67; col.11, ll.1-11):

a plurality of platforms communicatively coupled via an isochronous fabric, the platforms suitable for providing a logic function, the platforms including embedded programmable logic, memory and a reconfigurable core communicatively coupled (col.2, ll.26-38; col.8, ll.12-46; col.9, ll.34-50); and

a means for providing a map expressing availability of the plurality of platforms for performing a logic function (col.2, ll.54-67; col.3, ll.15-22; col.3, ll.58-67; col.4, ll.1-67; col.5, ll.1-2; col.8, ll.9-12; col.10, ll.53-67; col.11, ll.1-11),

wherein the platforms and the map are used for integrated circuit design (col.1, ll.53-67; col.2, ll.1-2; col.6, ll.32-38; col.7, ll.40-57).

As to claims 2-8, 10-14, 16-21 and 23-25 Athanas recites:

(2), (12), (16), (23) The system/method, wherein the map includes instruction set architecture extensions and embedded programmable logic core adjuncts (col.8, ll.27-29; col.10, ll.53-67; col.1, ll.1-11);

(3), (13), (17), (24) The system/method, wherein the map describes logic functions as provided by the plurality of platforms on a cycle-by-cycle basis (col.4, ll.53-67; col.5, ll.1-2);

(4), (14), (18), (25) The system/method, wherein the map describes logic functions as provided by the plurality of platforms in a manner so as to express groupings (combining) of platforms (col.6, ll.66-67; col.7, ll.1-12);

(5), (19) The system, wherein the embedded programmable logic includes at least one of programmable gate arrays, and programmable circuit elements definable from a stored representation (library) (col.8, ll.9-42; col.10, ll.53-67; col.11, ll.1-11);

(6), (20) The system, wherein the fabric interconnect is isochronous (col.8, ll.36-46; col.9, ll.34-50);

(7) The system as described in claim 1, wherein the plurality of platforms is communicatively coupled via a fabric interconnect that is isochronous (col.9, ll.34-50; col.9, ll.66-67; col.10, ll.1-22);

(8), (21) The system, wherein instruction set extensions are utilized through the use of the map to coordinate discrete instruction set extensions on a cycle-by-cycle basis and execution is synchronized across the plurality of platforms utilizing an

isochronous fabric interconnect (col.4, ll.17-67; col.5, ll.1-2; col.6, ll.66-67; col.7, ll.1-12; col.9, ll.34-50; col.9, ll.66-67; col.10, ll.1-22);

(10) The method as described in claim 9, wherein availability of the platforms is determined by referencing a map (col.10, ll.53-67; col.11, ll.1-11);

(11) The method as described in claim 10, wherein the map expresses logic functions of the plurality of platforms (col.3, ll.58-67; col.4, ll.1-67; col.5, ll.1-2; col.8, ll.9-12).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Master et al. (US Patent 6,836,839) describes integrated circuit embodiment that includes a plurality of heterogeneous computational elements coupled to an interconnection network. The plurality of heterogeneous computational elements include corresponding computational elements having fixed and differing architectures, such as fixed architectures for different functions such as memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability. In response to configuration information, the interconnection network is operative in real-time to configure and reconfigure the plurality of heterogeneous computational elements for a plurality of different functional modes, including linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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